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1. Detecting SEU-caused routing errors in SRAM-based FPGAs

Reddy, E.S.S.; Chandrasekhar, V.; Sashikanth, M.; Kamakoti, V.; Vijaykrishnan, N.;
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[AbstractPlus](#) | Full Text: [PDF\(120 KB\)](#) [IEEE CNF](#)[Rights and Permissions](#)**2. Multiple errors produced by single upsets in FPGA configuration memory: a possible solution**

Sonza Reorda, M.; Sterpone, L.; Violante, M.;
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Frantz, A.P.; Carro, L.; Cota, E.; Kastensmidt, F.L.;
[On-Line Testing Symposium, 2006. IOLTS 2006. 12th IEEE International](#)
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[AbstractPlus](#) | Full Text: [PDF\(160 KB\)](#) [IEEE CNF](#)[Rights and Permissions](#)**4. A new reliability-oriented place and route algorithm for SRAM-based FPGAs**

Sterpone, L.; Violante, M.;
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Volume 55, Issue 6, June 2006 Page(s):732 - 744
Digital Object Identifier 10.1109/TC.2006.82

[AbstractPlus](#) | Full Text: [PDF\(1888 KB\)](#) [IEEE JNL](#)[Rights and Permissions](#)**5. On the evaluation of SEU sensitiveness in SRAM-based FPGAs**

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13-16 March 2001 Page(s):219 - 223
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